

K1458LS 46-VB Datasheet

N-Channel 950 V (D-S) Power MOSFET

PRODUCT SUMMARY

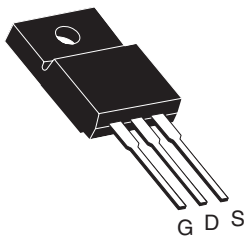
V_{DS} (V)	950	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	3.5
Q_g (Max.) (nC)	78	
Q_{gs} (nC)	10	
Q_{gd} (nC)	42	
Configuration	Single	

FEATURES

- Isolated Package
- High Voltage Isolation = 2.5 kV_{RMS} (t = 60 s; f = 60 Hz)
- Sink to Lead Creepage Distance = 4.8 mm
- Dynamic dV/dt Rating
- Low Thermal Resistance
- Lead (Pb)-free Available



RoHS*
COMPLIANT

TO-220 FULLPAK**N-Channel MOSFET****ABSOLUTE MAXIMUM RATINGS** $T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V _{DS}	950	V
Gate-Source Voltage			V _{GS}	± 20	
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	I _D	3.0	A
		T _C = 100 °C		2.3	
Pulsed Drain Current ^a			I _{DM}	10	
Linear Derating Factor				0.28	W/°C
Single Pulse Avalanche Energy ^b			E _{AS}	220	mJ
Repetitive Avalanche Current ^a			I _{AR}	1.9	A
Repetitive Avalanche Energy ^a			E _{AR}	3.5	mJ
Maximum Power Dissipation	T _C = 25 °C		P _D	35	W
Peak Diode Recovery dV/dt ^c			dV/dt	1.5	V/ns
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)		for 10 s		300 ^d	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

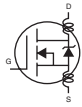

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 115\text{ mH}$, $R_G = 25\text{ }\Omega$, $I_{AS} = 1.9\text{ A}$ (see fig. 12).
- $I_{SD} \leq 3.6\text{ A}$, $dI/dt \leq 70\text{ A}/\mu\text{s}$, $V_{DD} \leq 600$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	65	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	3.6	

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		950	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	1.1	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 900 V, V _{GS} = 0 V		-	-	100	μA
		V _{DS} = 720 V, V _{GS} = 0 V, T _J = 125 °C		-	-	500	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 1.1 A ^b	-	3.5	-	Ω
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 1.1 A ^b		1.7	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	1200	-	pF
Output Capacitance	C _{oss}			-	320	-	
Reverse Transfer Capacitance	C _{rss}			-	200	-	
Drain to Sink Capacitance	C	f = 1.0 MHz		-	12	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 3.6 A, V _{DS} = 360 V, see fig. 6 and 13 ^b	-	-	78	nC
Gate-Source Charge	Q _{gs}			-	-	10	
Gate-Drain Charge	Q _{gd}			-	-	42	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 450 V, I _D = 3.6 A, R _G = 12 Ω, R _D = 120 Ω, see fig. 10 ^b		-	14	-	ns
Rise Time	t _r			-	25	-	
Turn-Off Delay Time	t _{d(off)}			-	90	-	
Fall Time	t _f			-	30	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	1.9	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	7.6	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 1.9 A, V _{GS} = 0 V ^b		-	-	1.8	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 3.6 A, dI/dt = 100 A/μs ^b		-	430	650	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	1.4	2.1	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
 b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

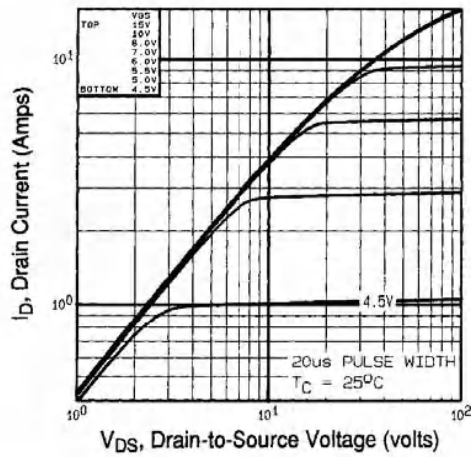
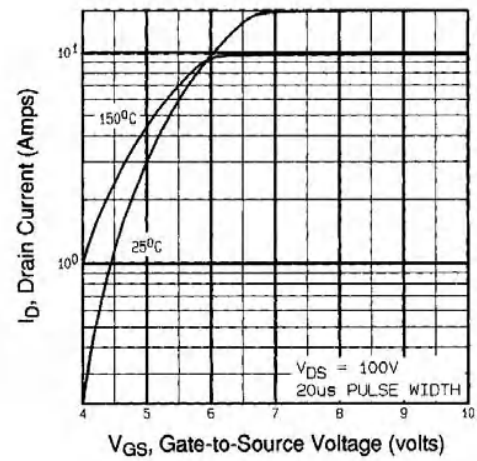
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted
Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^{\circ}\text{C}$ 

Fig. 3 - Typical Transfer Characteristics

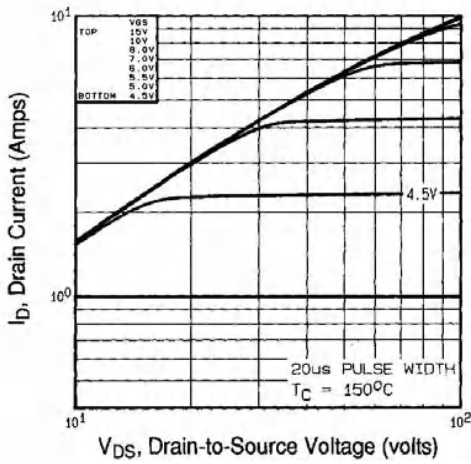
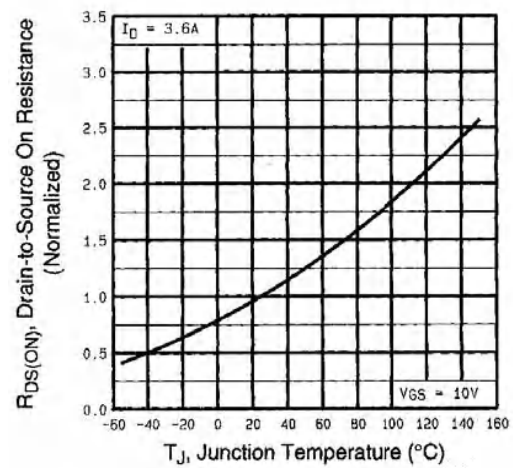
Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ }^{\circ}\text{C}$ 

Fig. 4 - Normalized On-Resistance vs. Temperature

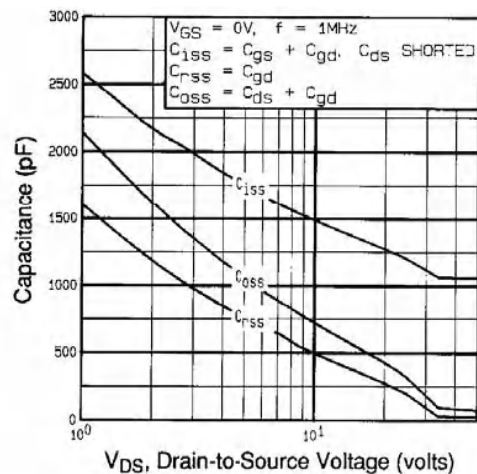


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

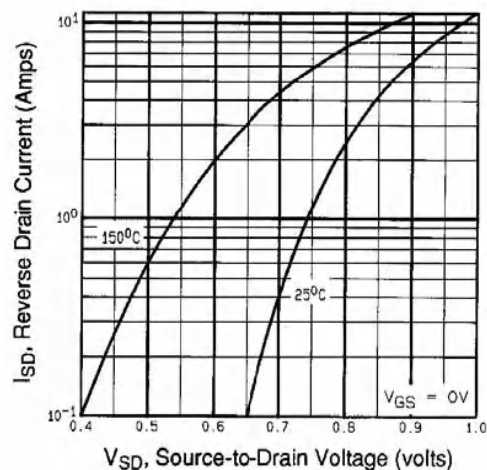


Fig. 7 - Typical Source-Drain Diode Forward Voltage

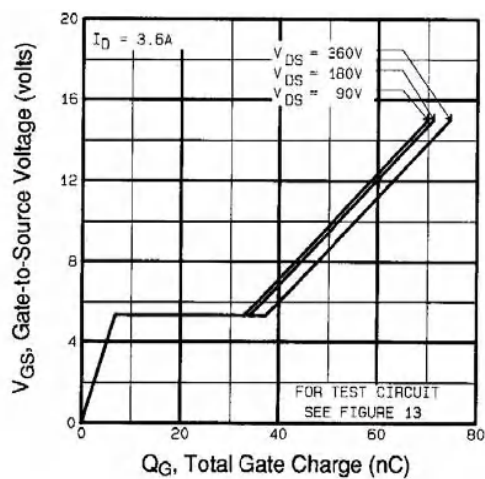


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

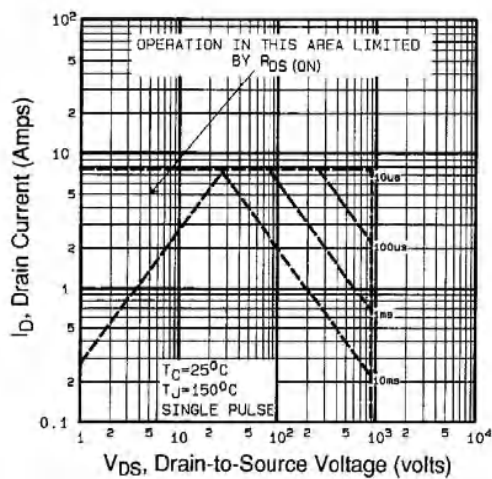


Fig. 8 - Maximum Safe Operating Area

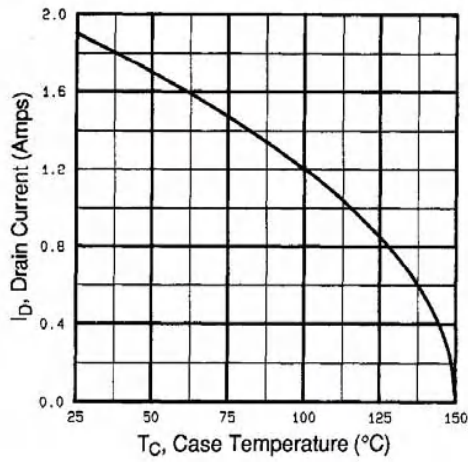


Fig. 9 - Maximum Drain Current vs. Case Temperature

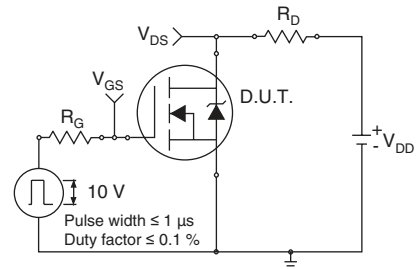


Fig. 10a - Switching Time Test Circuit

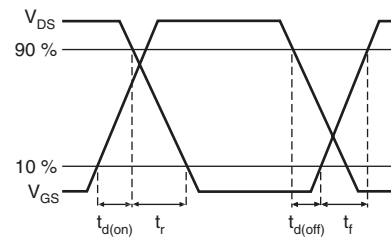


Fig. 10b - Switching Time Waveforms

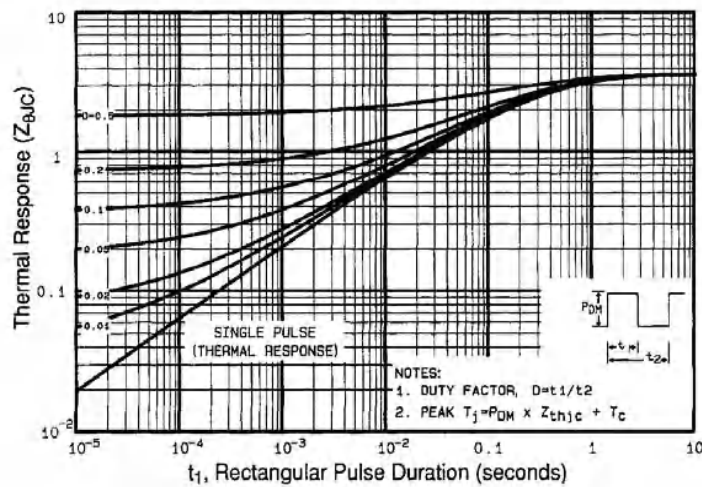


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

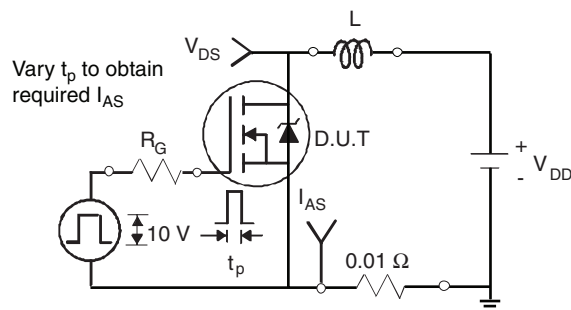


Fig. 12a - Unclamped Inductive Test Circuit



Fig. 12b - Unclamped Inductive Waveforms

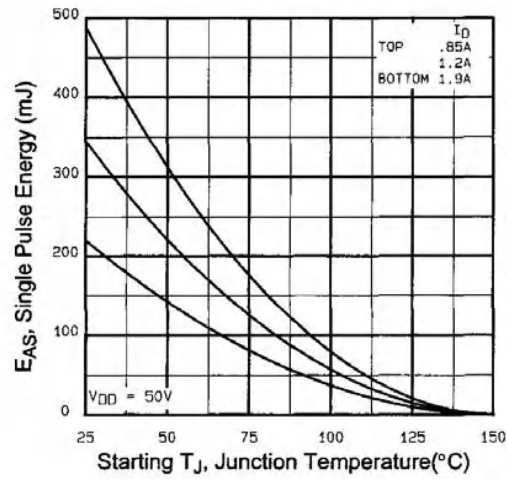


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

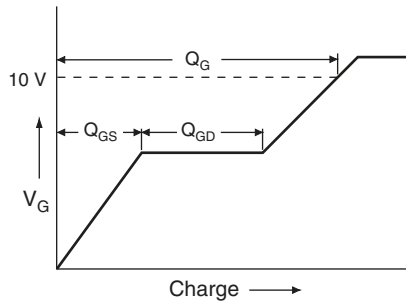


Fig. 13a - Basic Gate Charge Waveform

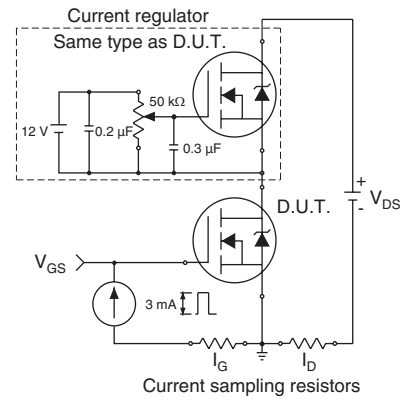


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

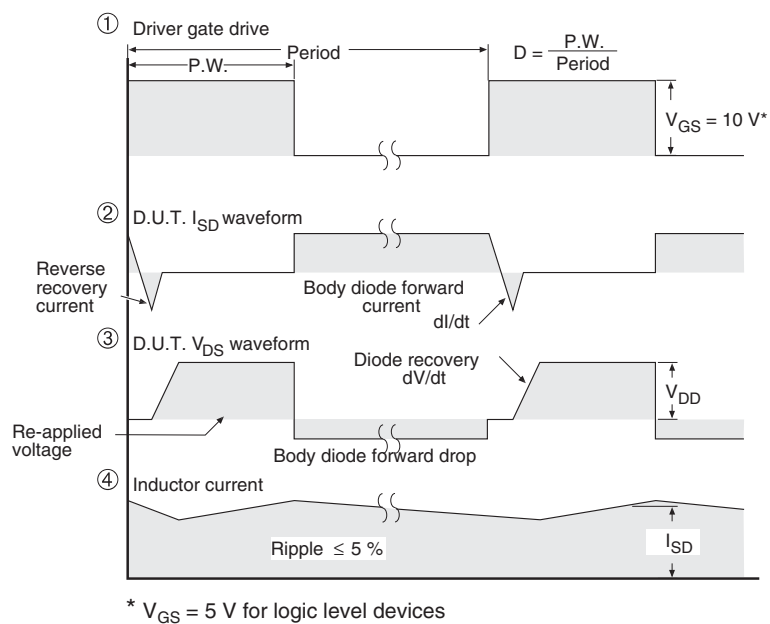
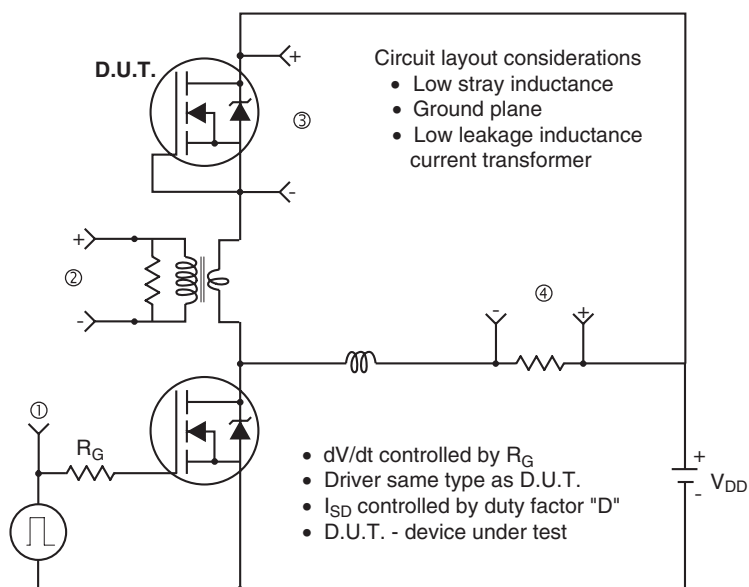
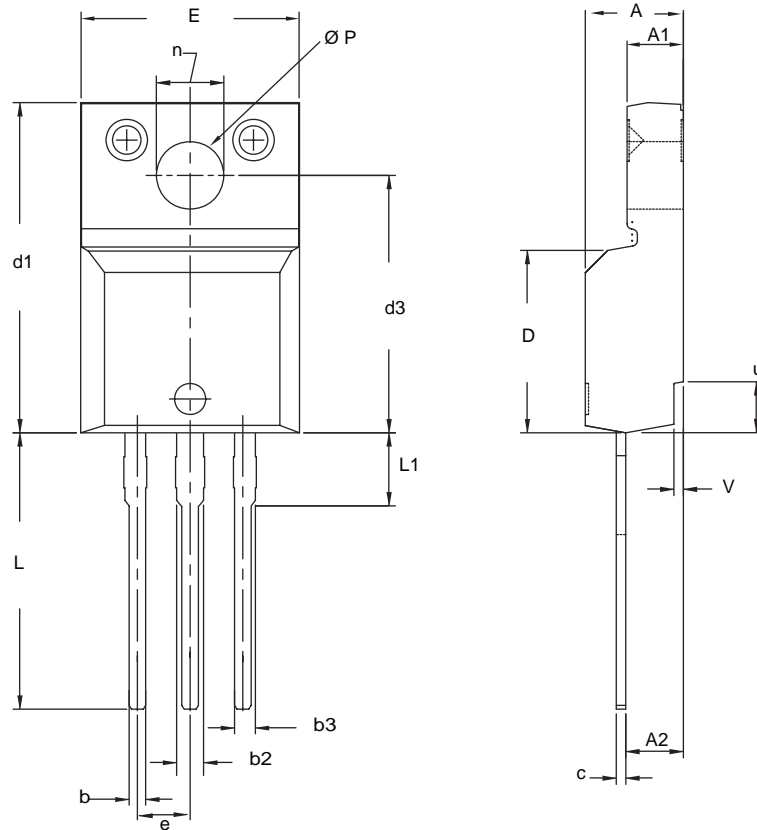


Fig.14 - For N-Channel

TO-220 FULLPAK (HIGH VOLTAGE)

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
v	0.400	0.500	0.016	0.020

ECN: X09-0126-Rev. B, 26-Oct-09
 DWG: 5972

Notes

1. To be used only for process drawing.
2. These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads.
3. All critical dimensions should C meet $C_{pk} > 1.33$.
4. All dimensions include burrs and plating thickness.
5. No chipping or package damage.

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